

SPECIFICATION AMENDMENTS

Please replace paragraph 21 of the published specification with the following:

The integrating unit 26 includes a switch 39 operated by the toggle unit 24, and a memory device 41 for providing the shift voltage $SV(t)$ to the shift amplifier 22. The memory device 41 includes a capacitive memory component 42 selectively strapped between the shift voltage limiter 27 and GND to provide the shift voltage $SV(t)$, and a resistive memory component 43 in parallel to the capacitive memory component 42. ON digital control states, on the condition that $I_{sub.N} > I_{sub.LED(t)}$, close the switch 39 for continuously charging the capacitive memory component 42 for continuously increasing the shift voltage $SV(t)$, up to the shift voltage $SV(t)$'s maximum value $SV_{sub.max}$, as determined by the shift voltage limiter 27 in the long absence of incoming digital data pulses. Conversely, OFF digital control states resulting from $I_{sub.LED(t)} > I_{sub.N}$ open the switch 39 to ~~slowly~~ swiftly discharge the capacitive memory component 42 to decrease the shift voltage $SV(t)$ via the resistive memory component 43.